Nomad: Non-Exclusive Memory Tiering via Transactional Page Migration

Speaker: Jiahao Li

Authors: Lingfeng Xiang, Zhen Lin, Weishu Deng, Hui Lu, Jia Rao, Yifan Yuan and Ren Wang

NUMA Systems





NUMA Systems





- I. Nodes are connected through inter-connections.
- 2. Accessing remote memory is more costly than accessing local memory.

New Memory Hierarchy





CXL enables more versatile memory hierarchy

NUMA Systems





5

Memory Tiering – Hardware Approach



DRAM becomes "L4" cache and NVM/CXL becomes main memory.

Memory Tiering – Hardware Approach



DRAM becomes "L4" cache and NVM/CXL becomes main memory.

Pros:

- I. Transparent.
- 2. Small granularity (cacheline).

Cons:

I. Hard-coded

2. Prone to cache conflicts. [Johnny Cache OSDI'23]

Memory Tiering – Software Approach

Page migration is used in exclusive memory tiering to speedup memory access:

- I. Migrate hot remote pages to application's local node.
- 2. Migrate cold pages to slower tier to make space for hot pages.



Memory Tiering – Challenges



- I. Which page to promote/demote?
- 2. Where to place the migrated pages?
- 3. How to migrate pages efficiently?



These methods are used to tracking page accesses:

- I. Page faults (Linux NUMA balancing)
 - Periodically make part of application's address space (256MB) inaccessible, page's hotness is indicated by whether page faults are triggered.
 - Faulted pages are considered hot and will be migrated to fast tier.



These methods are used to tracking page accesses:

- I. Page faults (Linux NUMA balancing)
- 2. Page Table Scanning (Linux kswapd)
 - Kernel maintains active and inactive LRU lists for each NUMA node.
 - Periodically scan all PTEs' access bits. If a PTE's access bit is set, the corresponding page will be moved to the active LRU.
 - Pages in inactive list are considered cold. When the memory is nearly full, they will be swapped out to swap space.



These methods are used to tracking page accesses:

- I. Page faults (Linux NUMA balancing)
- 2. Page Table Scanning (Linux kswapd)
- 3. Processor Event-based Sampling (HeMem SOSP'21)
 - Intel processor support event-based sampling to sample page access through certain events (e.g. MEM_LOAD_L3_MISS_RETIRED.LOCAL_DRAM).
 - Pages with larger access count are considered hot.





Memory Tiering – TPP



- I. Lightweight reclamation
 - Migration instead of swapping





- I. Lightweight reclamation
- 2. Decoupling allocation and reclamation

Memory Tiering – TPP



- I. Lightweight reclamation
- 2. Decoupling allocation and reclamation
- 3. New promotion strategy



Memory Tiering – TPP



- I. Lightweight reclamation
- 2. Decoupling allocation and reclamation
- 3. New promotion strategy
- 4. Page type-aware allocation

Page Migration is Complex



Page migration procedure:

- I. The system must trap to the kernel.
- 2. Lock the PTE of the migrating page and unmap it from page table.
- 3. TLB shootdown.
- 4. Copy the content of the page.
- 5. Remap the PTE.



An experiment to demonstrate TPP problems:

- Workload: memory access with Zipfian distribution
- Fast tier size: I6GB
- Working set size (WSS): I0GB / 24GB
- Allocation policy: frequency-opt / random, pre-allocating 10GB in fast tier to simulate memory usage of existing applications









Two problems in TPP:

I. Migration limit the application's memory access bandwidth.





Two problems in TPP:

- I. Migration limit the application's memory access bandwidth.
- 2. When WSS exceeds the capacity of the fast tier, TPP enters memory thrashing.



In TPP, promotion is synchronous



Synchronous promotion causes TPP performance degradation during migration





Goals:

- Enable the CPU to freely access both fast and slow memory
- Move page migration off the critical path of users' data access

NOMAD Approaches:

- Transactional page migration
- Non-exclusive tiering via page shadowing

New page

Old page

DSTC, CHINA



Flip bit

Page table entry

Design Overview

25



Major steps:

I. Clear the dirty bit in PTE



Issue a TLB shootdown. The page remains accessible



Major steps:

- I. Clear the dirty bit in PTE
- 2. Copy page





Major steps:

- I. Clear the dirty bit in PTE
- 2. Copy page
- 3. Unmap page



Issue second TLB shootdown. The page becomes inaccessible





4. Map the page to destination





4. Map the page to source and abort migration

Minimizing Page Faults





Linux batches (up to 15) LRU movements to reduce queue management overhead. In the worst case, migrating one page may generate as many as 15 page faults.

Minimizing Page Faults



- NOMAD introduces PCQ to record pages that faulted but not in the active list.
- Scan PTEs of pages in PCQ Kernel on every fault to decide space whether promote it to MPQ
- kpromote asynchronously performs TPM on pages in MPQ



CPU1

Page Shadowing



Page Shadowing **USTC, CHINA** Application load 0x7fff1234 NOMAD marks all master PFN 1 Promote PFN 0 pages as read-only CXL/PMem page **DRAM** page fast tier slow tier **PFNO** Page table entry 0 Shadow r/w Writeable

Application store 0x7fff1234 Restore writable bit on page PFN 1 Promote PFN 0 writes: CXL/PMem page DRAM page • No overhead for read-only pages • Single page fault for writable fast tier slow tier pages **PFNO** Page table entry 1 1 Writeable Shadow r/w

Page Shadowing

USTC, CHINA

Testbeds



- Intel CPU + 16 GB Intel FPGA-based CXL memory (CXL-FPGA)
- Intel CPU + 6 x 256GB Optane PMem (PMem)
- AMD CPU + 4 x 256GB Micron CXL memory (CXL-Product)
- DRAM: I6 GB





Testbed: CXL-FPGA



 NOMAD significantly outperforms TPP during active migration and for large WSS



Testbed: CXL-FPGA



 NOMAD significantly outperforms TPP during active migration and for large WSS 2. Sampling-based approach (Memtis) achieves stable
performance during
thrashing but fails to
optimally place hot data in
fast memory



Testbed: CXL-FPGA



TPP Memtis-default NOMAD (SUM) 4000 4000 2000 Read Migration stable Migration in progress Migration stable

Large WSS

Small WSS

 NOMAD significantly outperforms TPP during active migration and for large WSS 2. Sampling-based approach (Memtis) achieves stable
performance during
thrashing but fails to
optimally place hot data in
fast memory 3. NOMAD is more effective for read-only workloads and suffers from migration abortions for write-intensive workloads



Testbed: PMem



thanks to a lack of migrations, its latency is suboptimal, suggesting page migration is ineffective

Real-world Applications - Redis

Testbed: CXL-FPGA

Case I: I3GB RSS, demote pages

Case 2: 24GB RSS, demote pages

Case 3: 24GB RSS, no demotion



NOMAD outperforms TPP in all cases and outperforms Memtis when WSS fits in fast tier.

Real-world Applications - Redis

Testbed: CXL-FPGA

Case I: I3GB RSS, demote pages

Case 2: 24GB RSS, demote pages

Case 3: 24GB RSS, no demotion



Page migration could incur nontrivial overhead, and a strategy to dynamically switch it on/off is needed.

Real-world Applications - liblinear





1. Page fault-based approaches outperform Memtis and nomigration for small RSS

Real-world Applications - liblinear





 Page fault-based approaches outperform Memtis and nomigration for small RSS TPP's performance significantly declines due to inefficient migration.

Conclusions



NOMAD is a tiered memory management mechanism that features:

- Transactional page migration
- Page shadowing
- Non-exclusive memory tiering

Results show that NOMAD is significantly more efficient than the state-of-the- art tiered memory management scheme in Linux but call for more research on memory tiering

• The optimal strategy to enable/disable page migrations under high memory pressure